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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
( Not for submission under 37 CFR 1.99)

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| Application Number     | 09989762         |
| Filing Date            | 2001-11-19       |
| First Named Inventor   | Kenneth Y. Ogami |
| Art Unit               | 2123             |
| Examiner Name          | Osborne, Luke R. |
| Attorney Docket Number | CD01175M         |

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| 49 | 6043719 | B1 | 2000-03-28 | Lin et al.         | Entire Document |
| 50 | 6732347 | B1 | 2004-05-04 | Camilleri et al.   | Entire Document |

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| Application Number     | 09989762         |
| Filing Date            | 2001-11-19       |
| First Named Inventor   | Kenneth Y. Ogami |
| Art Unit               | 2123             |
| Examiner Name          | Osborne, Luke R. |
| Attorney Docket Number | CD01175M         |

|   |             |    |            |       |                 |
|---|-------------|----|------------|-------|-----------------|
| 1 | 20050280453 | A1 | 2005-12-22 | Hsieh | Entire Document |
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|--------------------|---------|---|--------------------------|
|                    | 1       | Application Number 10/226,911 (CD02112): "Calibration of Integrated Circuit Time Constants," Gehring et al., 32 pages   | <input type="checkbox"/> |
|                    | 2       | USPTO Notice of Allowance for Application Number 09/943,149 (CD01085) dated 01/12/2004; 7 pages   | <input type="checkbox"/> |
|                    | 3       | USPTO Non-Final Rejection for Application Number 09/943,149 (CD01085) dated 08/28/2003; 9 pages   | <input type="checkbox"/> |
|                    | 4       | USPTO Final Rejection for Application Number 09/943,149 (CD01085) dated 05/07/2003; 10 pages  | <input type="checkbox"/> |
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|----|--|--------------------------|
| 6  | Application Number 09/943,149 (CD01085): "Method for Phase Locking in a Phase Lock Loop," Moyal et al.; 21 pages   | <input type="checkbox"/> |
| 7  | Durham et al., "Integrated Continuous-Time Balanced Filters for 16-bit DSP Interfaces," IEEE, 1993; 6 pages  | <input type="checkbox"/> |
| 8  | Durham et al., "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," IEEE, 1992; 7 pages  | <input type="checkbox"/> |
| 9  | Durham et al., "High-Linearity Continuous-Time Filter in 5-V VLSI CMOS," IEEE, 1992; 8 pages   | <input type="checkbox"/> |
| 10 | Application Number 09/047,595 (CD97115): "Roving Range Control to Limit Receive PLL Frequency of Operation," Scott; 35 pages                                 | <input type="checkbox"/> |
| 11 | Application Number 09/216,460 (CD98099): "Circuit and Method for Controlling an Output of a Ring Oscillator," Abugharbieh et al.; 21 pages                   | <input type="checkbox"/> |
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| 13 | Application Number 09/471,576 (CD99062): "Reference-Free Clock Generation and Data Recovery PLL," Dalmia; 30 pages   | <input type="checkbox"/> |
| 14 | Application Number 10/083,442 (CD01264): "Method/Architecture for a Low Gain PLL with Wide Frequency Range," Meyers et al.; 28 pages                         | <input type="checkbox"/> |
| 15 | Application Number 09/470,665 (CD99065): "Digital Phase/Frequency Detector, and Clock Generator and Data Recovery PLL Containing the Same," Dalmia; 26 pages | <input type="checkbox"/> |
| 16 | Application Number 09/893,161 (CD00094): "Architecture of a PLL with Dynamic Frequency Control on a PLD," Moore; 32 pages                                    | <input type="checkbox"/> |

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| Attorney Docket Number | CD01175M         |

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| 17 | Application Number 09/608,753 (CD00018): "PLL Lockout Watchdog," Wilson et al.; 24 pages   | <input type="checkbox"/> |
| 18 | Application Number 09/398,956 (CD99049): "Frequency Acquisition Rate Control in Phase Lock Loop Circuits," Moyal et al.; 35 pages  | <input type="checkbox"/> |
| 19 | Application Number 09/747,262 (CD00085): "Linearized Digital Phase-Locked Loop," Williams et al.; 9 pages  | <input type="checkbox"/> |
| 20 | Application Number 09/981,448 (CD01102): "Oscillator Tuning Method," Hauck; 28 pages   | <input type="checkbox"/> |
| 21 | Application Number 09/538,989 (CD98104): "Memory Based Phase Locked Loop," Krishnan; 27 pages  | <input type="checkbox"/> |
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| 23 | Application Number 08/865,342 (CD95045C): "Programmable Clock Generator," Mann et al.; 41 pages  | <input type="checkbox"/> |
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| 25 | USPTO Non-Final Rejection for Application Number 10/293,392 (CD02135) dated 10/16/2003; 6 pages  | <input type="checkbox"/> |
| 26 | Application Number 10/293,392 (CD02135): "Low Voltage Receiver Circuit and Method for Shifting the Differential Input Signals of the Receiver Depending on a Common Mode Voltage of the Input Signals," Maher et al.; 20 pages | <input type="checkbox"/> |
| 27 | USPTO Notice of Allowance for Application Number 10/288,003 (CD02108) dated 01/14/2005; 6 pages  | <input type="checkbox"/> |

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| Attorney Docket Number | CD01175M         |

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| 28 | USPTO Final Rejection for Application Number 10/288,003 (CD02108) dated 10/06/2004; 6 pages                                  | <input type="checkbox"/> |
| 29 | USPTO Non-Final Rejection for Application Number 10/288,003 (CD02108) dated 04/07/2004; 9 pages                              | <input type="checkbox"/> |
| 30 | Application Number 10/288,003 (CD02108): "Low Voltage Differential Signal Driver Circuit and Method," Roper et al.; 30 pages | <input type="checkbox"/> |
| 31 | USPTO Notice of Allowance for Application Number 09/989,777 (CD01208M) dated 06/09/2009; 7 pages                             | <input type="checkbox"/> |

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